Application Note 2722
Interfacing the DS2156 UTOPIA II Bus to Dallas Demo Kits

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INTRODUCTION

This application note describes how to use the DS2156 UTOPIA II bus interface on the Dallas Semiconductor DS2156DK development kit with either of the DK101 or DK2000 demo kit motherboards.

The DS2156 is user configurable for a TDM or UTOPIA II bus interface. The UTOPIA II interface has the following characteristics:

- Full or fractional DS1/E1 with bit rates in multiples of 64kbps
- Clear-channel E1
- Compliant to the ATM forum specifications for ATM over DS1 and E1
- Standard UTOPIA II interface to the ATM layer
- Configurable UTOPIA address
- Physical layer interface capable of accepting DS1/E1 stream in the form of either
  - Clock, data, and frame overhead indication
  - Gapped clock on data position
- Diagnostic loopback
- Transmit FIFO depth configurable to either 2, 3, or 4 cells deep
- Transmit FIFO depth indication for 2-cell space
- Optional single-bit HEC error insertion
- Programmable loss-of-cell delineation (LCD) integration and optional interrupt
- Interrupt for FIFO overrun in receive direction

The DK101 is a low-cost demo kit motherboard for evaluating Dallas Semiconductor Telecom ICs. The ICs are mounted on daughter cards specifically designed to plug into the DK101's connector. The DK101 provides a microprocessor; flash and SRAM-based program memory; various oscillators and support logic; and an RS-232 interface to a host PC. The processor runs general-purpose firmware that executes reads and writes to the daughter card on behalf of PC-based demo software.

The high-performance demo kit motherboard (DK2000) contains all the necessary support logic to completely evaluate the telecom daughter cards made by Dallas Semiconductor. DK2000 allows for prototyping and development by supplying the processor interface to various telecom products. Incorporating the MPC8260, 64MB of RAM, up to 1MB of L2-Cache, two banks of flash at 2MB each, fast Ethernet, and RS232, the DK2000 is powerful and flexible. The DK2000 provides each of the up to four daughter cards with processor bus interfaces, TDM and UTOPIA interfaces in the form of three 50-position high-density daughter card connectors.

THE DS2156 UTOPIA HARDWARE

The DS2156 has a user-selectable TDM or UTOPIA backplane. When the UTOPIA II backplane is enabled, the basic TDM signals such as clock, sync, and data are available in both the transmit and receive directions.

In an ATM application, a UTOPIA II bus interface is enabled via the TUSEL pin. When TUSEL is low, the TDM backplane is enabled, and when the TUSEL pin is set high, the UTOPIA II backplane is enabled. Each pin associated with the UTOPIA II bus interface is described.

UR-ADDR0–UR-ADDR4, **Receive UTOPIA Address**, **(Input):** This 5-bit UTOPIA address bus is driven from the ATM layer to select the appropriate UTOPIA port. RX_UTOP_ADDR4 is the MSB and RX_UTOP_ADDR0 is the LSB.

$\overline{\text{UR-ENB}}$, **Receive UTOPIA Enable, (Input):** This is an active-low signal asserted by the ATM layer to indicate that UR-DATAx and UR-SOC will be sampled at the end of the next cycle.

UR-SOC, **Receive UTOPIA Start of Cell (Output):** This active-high signal is asserted by the DS2156 when UR-DATAx contains the first valid byte of a cell, and is enabled only in cycles following those with $\overline{\text{UR-ENB}}$ asserted and cell transfer is in progress.

UR-DATA0–UR-DATA7, **Receive UTOPIA Data Bus (Output):** This byte-wide data bus is driven by the DS2156 in response to the selection of one of the UTOPIA ports by the ATM layer for cell transfer. This bus is tri-statable, and is enabled only in cycles following those with $\overline{\text{UR-ENB}}$ asserted and cell transfer is in progress for a port. UR-DATA7 is the MSB and UR-DATA0 is the LSB.

UR-CLAV, **Receive UTOPIA Cell Available (Output):** The active high UR-CLAV signal is asserted if a complete cell is available for transfer to the ATM layer for the polled port. If UR-ADDRx does not match with any one of UTOPIA port addresses, this signal will be tri-stated at the chip level using the control lines detailed below. UR-CLAV0 is driven in multiplexed with 1CLAV polling mode as well as direct status mode.

UR-CLK, **Receive UTOPIA Clock (Input):** Receive UTOPIA bus clock.

UT-ADDR0–UT-ADDR4, **Transmit UTOPIA Address (Input):** This 5-bit-wide bus is driven by the ATM layer to poll and select the appropriate UTOPIA port. UTADDR4 is the MSB and UT-ADDR0 is the LSB.

$\overline{\text{UT-ENB}}$, **Transmit UTOPIA Enable (Input):** Active-low enable signal asserted by ATM layer during cycles when UT-DATAx contains valid cell data.

UT-SOC, **Transmit UTOPIA Start of Cell (Input):** Active-high signal asserted by ATM layer when UT-DATAx contains the first valid byte of the cell.

UT-DATA0–UT-DATA7, **Transmit UTOPIA Data Bus (Input):** Byte-wide true data driven from ATM layer to one of the selected ports. UT-DATA7 is the MSB and UTDATA0 is the LSB.

UT-CLAV, **Transmit UTOPIA Cell Available (Output):** The active-high UT-CLAV signal is asserted by the DS2156 if it has a cell space available to accommodate a complete cell from the ATM layer to the polled port. If UT-ADDRx does not match with any one of UTOPIA port addresses, this signal should be tri-stated at the chip level using the control signals detailed below. UT-CLAV0 is driven in multiplexed with 1CLAV polling mode as well as direct status mode.

UT-2CLAV, **Transmit UTOPIA 2 Cells Available (Output):** This active-high signal is asserted by the DS2156 to indicate that the transmitter can accommodate 2 cells. UT-2CLAV0 is driven in multiplexed with 1CLAV mode as well as direct status mode for port 0. The timing of this signal follows as that of UT-CLAV. This bus is not tri-statable.

UT-UTDO, **UTOPIA Transmit Data Output (Output):** Access to the data prior to the transmit formatter. Updated on the rising edge of TCLK. This output is normally connected to TDATA.

UT-CLK, Transmit UTOPIA Clock (Input): Transmit UTOPIA bus clock.

UTOPIA BACKPLANE INTERFACE

The DS2156's UTOPIA interface maps the transmit ATM cells in a DS1/E1 frame as per ATM Forum specifications af-phy-0016.000 and af-phy-0064.000 and receives them in a similar mapping. On the receive side, the cell delineation mechanism used for finding ATM cell boundaries is performed as per ITU-T I.432. The terms ATM layer and system side are used synonymously and refer to the UTOPIA II interface of the DS2156.

UTOPIA—TRANSMIT OPERATION

The DS2156 interface to the ATM layer is fully compliant to the ATM Forum's UTOPIA Level 2 specification. Both direct status and multiplexed with 1CLAV modes are supported. The DS2156 can be configured to use any address from 0 to 31 as its UTOPIA port address, and has a 4-cell buffer for cell-rate decoupling.

The depth of the transmit FIFO is configurable to 2, 3, or 4 cells. When a port is polled and has cell space available, the DS2156 generates a cell available signal for that port. Additionally, the DS2156 generates a 2-cell space availability indication for each port. The DS2156 uses UT-SOC (transmit UTOPIA start of cell) to detect the first byte of a cell. If a spurious UT-SOC occurs during a cell transfer, then the DS2156 aligns with the latest UT-SOC and ignores the partial cell in the FIFO.

UTOPIA—RECEIVE OPERATION

The receive interface of the DS2156 is fully compliant to the ATM Forum's UTOPIA Level 2 Specifications. The DS2156 can be configured to use any one of address ranges 0 to 7, 8 to 15, 16 to 23, and 24 to 32 as UTOPIA port addresses. For direct status polling, the address range can be one of 0 to 3, 8 to 11, 16 to 19, and 24 to 27.

If the receive FIFO is not empty, the cell available signal is asserted. After a cell is transferred from the port, the external cell available signal will be updated based on receive FIFO fill level after one clock cycle from cell transfer completion. During this clock cycle, the cell available indication for the port is kept in the deasserted state. A one clock minimum latency between two cell transfers from the same UTOPIA port is needed by the DS2156 to update its internal cell pointers.

DS2156DK I/O PIN MAPPING TO CONNECT WITH ADTECH AX/4000

Table 1 shows how to connect the DS2156DK to an Adtech AX/4000 Broadband Test System to test the DS2156 UTOPIA II Bus.

Table 1. I/O Pin Mapping to Connect with ADTECH AX/4000

ADTECH TX PIN NUMBERS	ADTECH TX PIN NAMES	DS2156DK PIN NAMES	ADTECH RX PIN NUMBERS	ADTECH RX PIN NAMES	DS2156DK PIN NAMES
1	TXDATA_0	TNEGI	1	RXDATA_0	RLINK
2	TXDATA_1	TCLKI	2	RXDATA_1	RLCLK
3	TXDATA_2	TCLKO	3	RXDATA_2	RPOSI
4	TXDATA_3	TNEGO	4	RXDATA_3	RNEGI
6	TXDATA_4	TPOSO	6	RXDATA_4	RCLKI
7	TXDATA_5	TSER	7	RXDATA_5	RCLKO
8	TXDATA_6	TSIG	8	RXDATA_6	RNEGO
9	TXDATA_7	TSYSCLK	9	RXDATA_7	RPOSO
5, 10, 20, 25, 30	GND	GND	5, 10, 20, 40, 45	GND	GND
22	TXSOC	UOP0	22	RXSOC	RCHBLK
23	TXADDR0	UOP3	37	RXADDR0	RCHCLK
24	TXADDR1	TCHBLK	38	RXADDR1	RSIGF
26	TXADDR2	TLCLK	39	RXADDR2	RSIG
27	TXADDR3	TLINK	41	RXADDR3	RMSYNC
28	TXADDR4	TPOSI	42	RXADDR4	RFSYNC
29	TXCLAV0	LIUC	43	RXCLAV0	RSER
34	TXENABLE	UOP1	48	RXENB	BPCLK
36	UT_CLK	TSSYNC	49	UR_CLK	TCHCLK

UTOPIA II CONFIGURATION USING DS2156

The register settings in Table 2 configure the DS2156 daughter card for UTOPIA II, single CLAV, 8-bit mode on PHY port 0. UTOPIA II bus connection is provided by header J1 (Tx) and header J2 (Rx) on the DS2156DK.

After configuring the registers, the user needs to toggle the MSTREG.URST bit to reset the UTOPIA II core.

Table 2. UTOPIA II Setup, Register Settings for Daughter Card CPLD

NAME	VALUE		NAME	VALUE
SWITCH 1	0x0F		SWITCH 4	0x0F
SWITCH 2	0x03		LEVELS	0x07
SWITCH 3	0x0F			

Table 3 shows the register settings to configure the DS2156 to E1 mode of operation.

Table 3. UTOPIA II Setup, Register Settings for E1 Configuration

NAME	VALUE		NAME	VALUE
MSTREG	0x02		LBCR	0x00
E1RCR1	0x68		TAF	0x9B
E1RCR2	0x00		TNAF	0xC0
E1TCR1	0x15		LIC1	0x11
E1TCR2	0x00		LIC2	0x90
CCR1	0x00		LIC3	0x00
CCR4	0x00		LIC4	0x00
IOCR1	0x00			
IOCR2	0x00			

Table 4 shows the register settings to configure the DS2156 for UTOPIA II.

Table 4. UTOPIA II Setup, Register Settings for UTOPIA II Configuration

NAME	VALUE		NAME	VALUE
U_TCFR	0x01		U_RCR2	0x0
U_TCR1	0x05		U_TIUPB	0x0
U_TCR2	0x00		PCPR	0x22
U_RCFR	0x01		PCDR1–4	0x0
U_RCR1	0x01			

UTOPIA II SETUP: SETTING UP DS2156DK WITH ADTECH AX/4000

When the DS2156DK is connected with an Adtech AX/4000, the UTOPIA II configuration can be changed using the UTOPIA Level II setup interface on the computer running the Adtech AX/4000 software.

Figure 1 shows what the user will view to configure the UTOPIA II using the Adtech AX/4000 software.

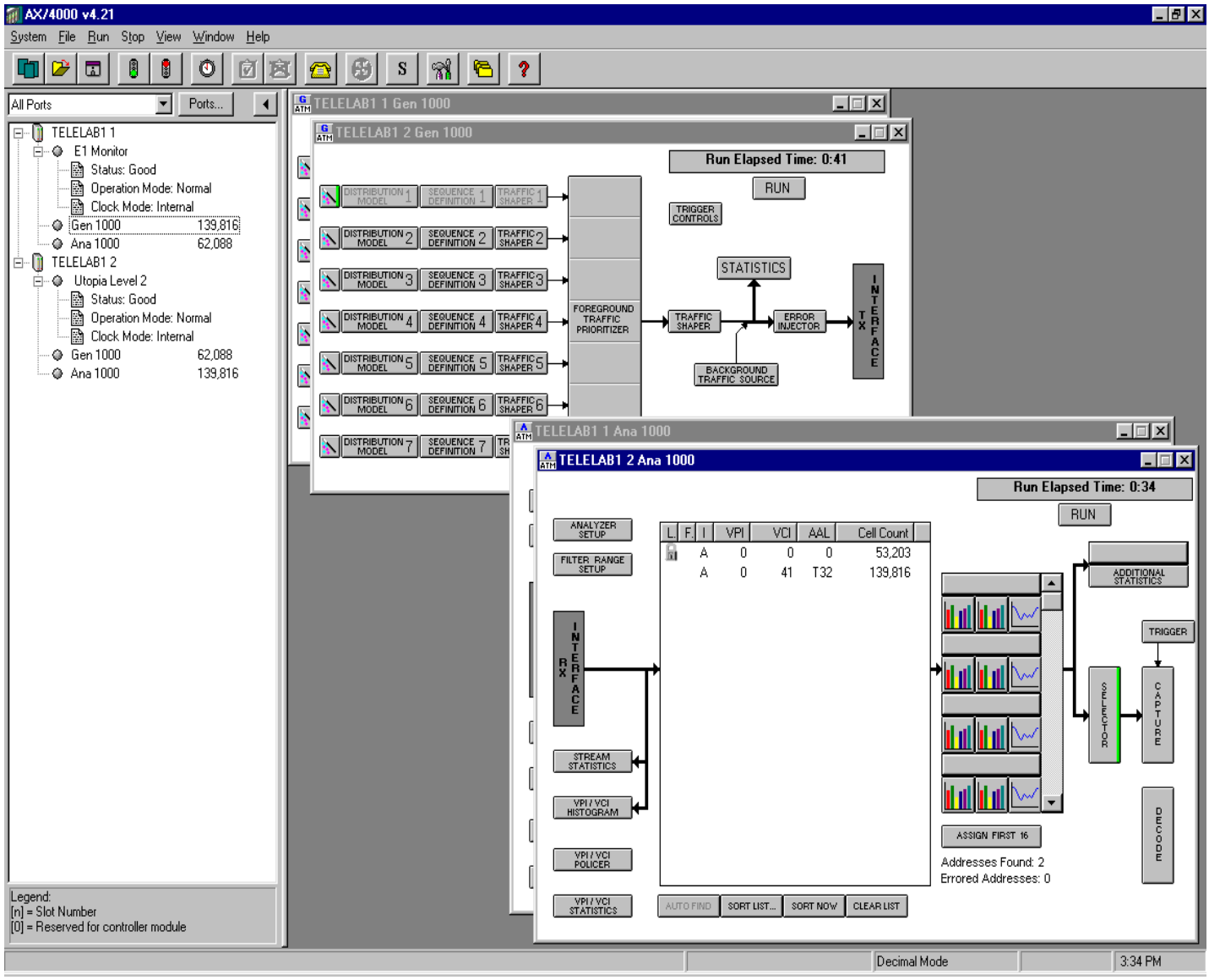

Figure 1. Adtech AX/4000 Software Interface

To change the setup for UTOPIA II, the user will view the interface that is shown in Figure 2.

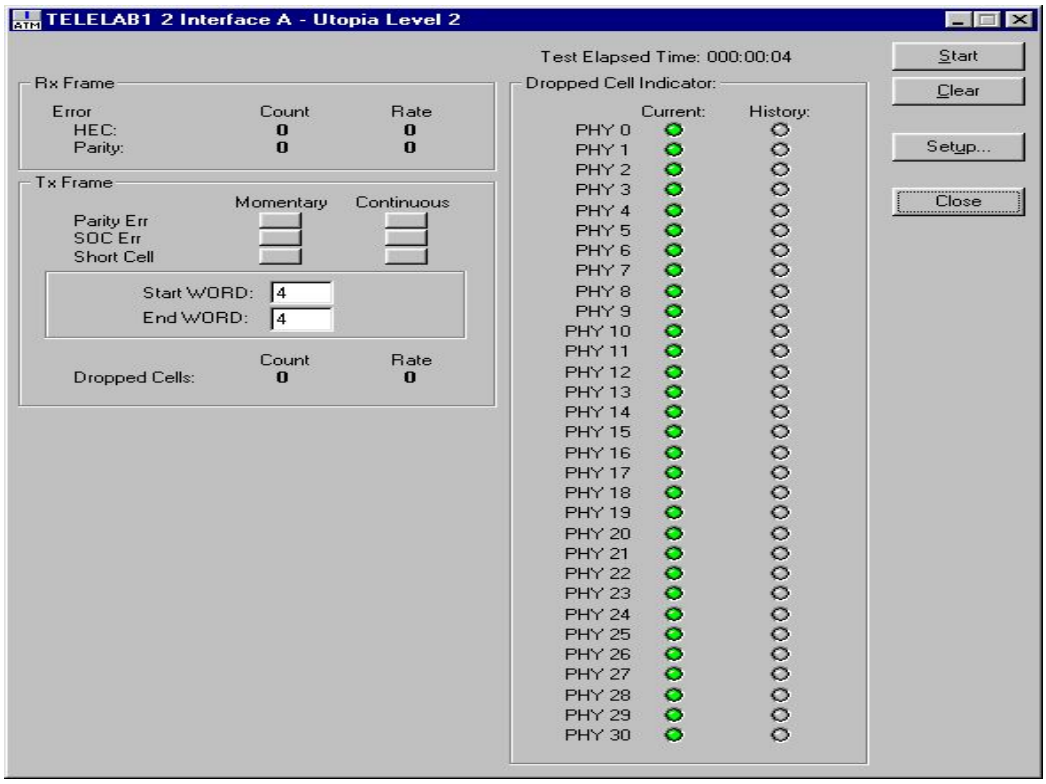

Figure 2. Adtech AX/4000 Software Interface for UTOPIA II

By clicking on the SETUP box, the following functions are accessed from the UTOPIA II setup dialog box. Figure 3 shows the General Mode.

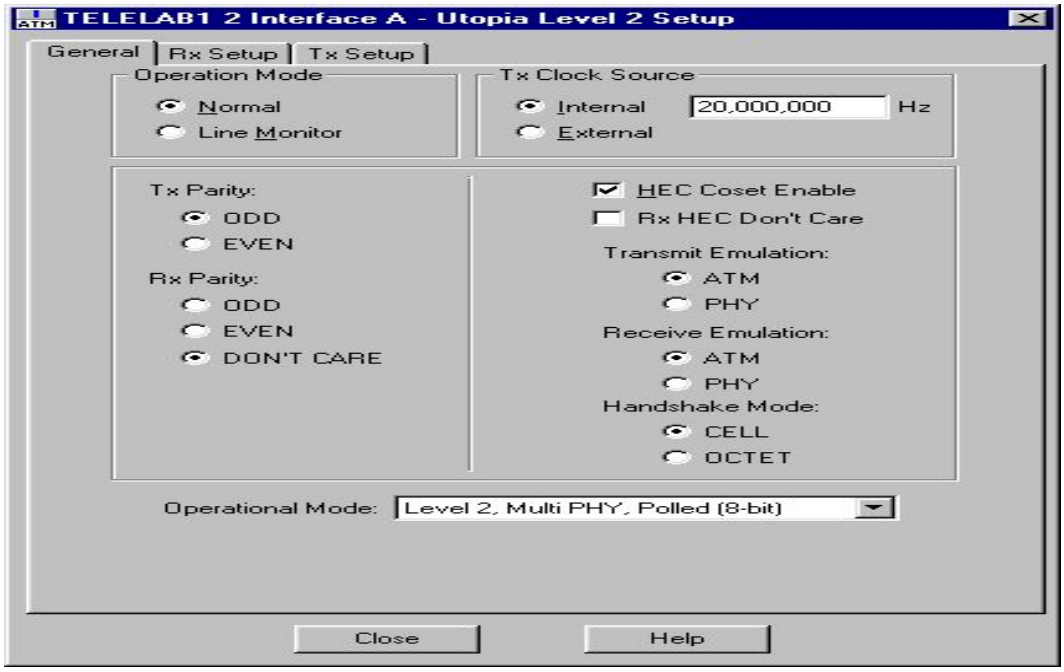

Figure 3. Adtech AX/4000 Software Interface for UTOPIA II Setup on General Mode

To change the receive and transmit setup, there are ‘Rx Setup’ and ‘Tx Setup’ in the software interface. Figures 4 and 5 show the software interface on the receive and the transmit setup, respectively.

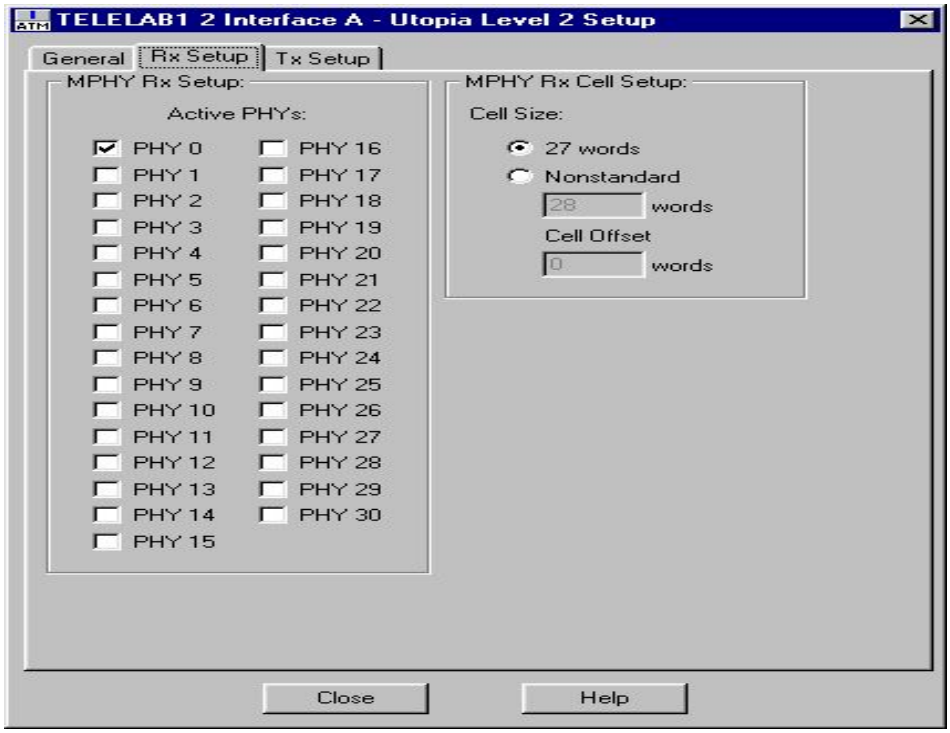

Figure 4. Adtech AX/4000 Software Interface for UTOPIA II Setup on Receive Mode

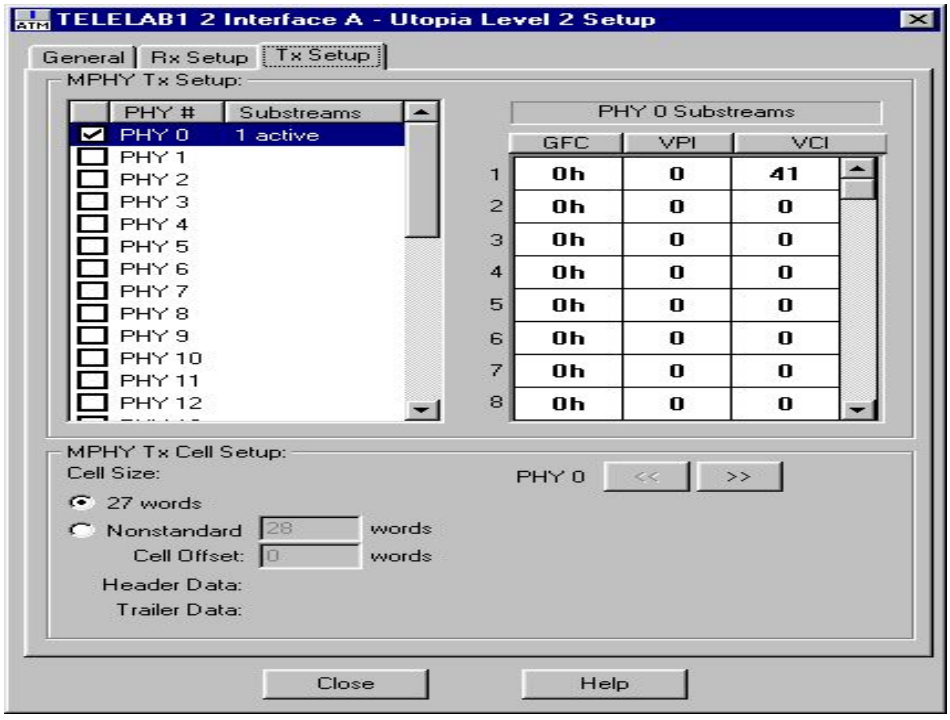

Figure 5. Adtech AX/4000 Software Interface for UTOPIA II Setup on Transmit Mode

DK2000

The DK2000 development platform has 4MB of flash memory organized into two banks. Each bank is organized as 512k x 32, consisting of four Atmel AT49LV040 devices that are socketed for easy removal and external programming. Using jumpers, either of the two flash banks can be configured as the boot ROM. The flash banks are controlled by the MPC8260's chip select 0 and 1. The chip select assignment for each bank is a jumper configurable selection. The board's silkscreen marks which byte lane each FLASH device is attached to.

To satisfy debug and development needs, the DK2000 platform provides two debug connectors. Connector P9 is a standard JTAG/COP interface to the MPC8260 as defined by Motorola. Connector P20 is a Vision Probe/Vision ICE connector as defined by WindRiver.

User software may be downloaded to the onboard SRAM or FLASH using either the Vision ICE port or the JTAG/COP port. If FLASH programming is preferred then FLASH bank 1 is recommended as FLASH bank 0 contains the default firmware.

MPC8260 I/O PIN MAPPING

The MPC8260 provides 120 I/O pins that can be configured for special purpose or for general purpose I/O. The DK2000 development platform takes advantage of as much of the I/O capability as possible.

To connect the DS2156DK daughter card to a DK2000, just plug the DS2156DK daughter card into one of the DK2000's daughter card connectors. Some daughter cards have two connectors while others have three. The third connector, which is optional, is for advanced features (UTOPIA bus, POS-PHY bus, etc). The DK2000 is compatible with both two-connector and three-connector daughter cards, and supports the advanced features available on the third connector. Note that daughter cards are not designed for hot insertion; only connect daughter cards to the DK2000 platform with the power off. Table 1 describes the pin configuration on the processor MPC8260 for UTOPIA and how they are connected through the daughter Card connectors.

Table 5. I/O Pin Assignments for UTOPIA

UTOPIA FUNCTION	SIGNAL NAMES ON THE PROCESSOR MPC8260	PIN NUMBERS ON DAUGHTER CARD
TXENA	PA31	16
TXCLAV0	PA30	23
TXSOC	PA29	17
RXENA	PA28	42
RXSOC	PA27	43
RXCLAV0	PA26	49
TXD0	PA25	13, 17
TXD1	PA24	14
TXD2	PA23	11
TXD3	PA22	12
TXD4	PA21	9
TXD5	PA20	10
TXD6	PA19	7
UTOPIA function	Signal names on the MPC8260 processor	Pin numbers on daughter card
TXD7	PA18	8
RXD7	PA17	34
RXD6	PA16	33
RXD5	PA15	36
RXD4	PA14	35
RXD3	PA13	38
RXD2	PA12	37
RXD1	PA11	40
RXD0	PA10	39
TXCLK	PC21	18
RXCLK	PC20	44
TXADDR0	PC15	6
RXADDR0	PC14	32
TXADDR1	PC13	3
RXADDR1	PC12	29
TXADDR2/TXCLAV1	PC7	4, 24
RXADDR2/RXCLAV1	PC6	30, 50
RXADDR3/RXCLAV2	PD29	27, 47
TXADDR4/CLAV3	PD19	2, 22
RXADDR4/RXCLAV3	PD18	28, 48
RXPRTY	PD17	41
TXADDR3/TXCLAV2	PD7	1, 21
TXPRTY	EPLD (generated in logic)	15

FOR MORE INFORMATION

For more information on the UTOPIA/DS2156, DK101, or DK2000, visit our website www.maxim-ic.com/telecom or contact the Dallas Semiconductor Telecommunication Applications support team via email at telecom.support@dalsemi.com.